

JTAG Extension Addresses New Bus Structures

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Boundary-scan (aka JTAG, IEEE Std. 1149.1) testing has now been with us in principle for almost two decades. During this time the technique has been used widely throughout the 'high tech' industries to test, debug and program high-performance digital circuits. Typical markets have included automotive electronics, broadcast, datacoms, defence, medical & telecoms, industries. However, whilst this system has enjoyed considerable success in testing 'restricted access' pcb's populated with fine-pitched and BGA parts new bus structure have contrived to limit its usefulness in some applications.

Boundary-scan Basics.

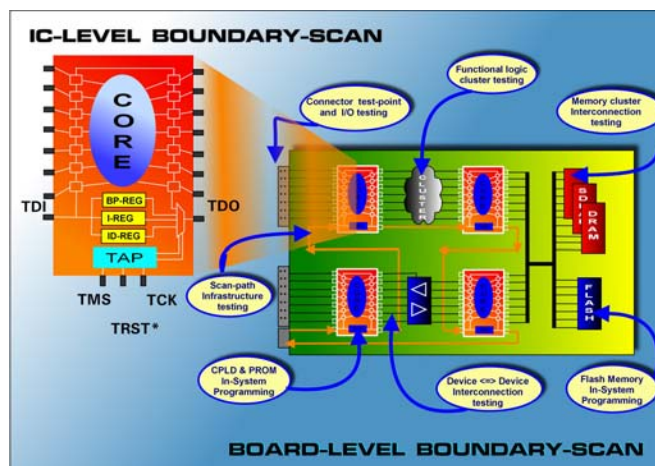
Originally intended as an aid to PCB production test, boundary-scan circuitry has been implemented in literally thousands of devices since its inception in 1990 and additions to the standard have enhanced its capabilities ever since. The basic idea is simple enough – embed test 'cells' comprising latches and multiplexors into a digital or mixed signal part that can drive or capture a logic signal at the device pins, and access these via a serial scan chain or multiple I/O shift register. By adding a state machine known as the JTAG TAP (Test Access Port) controller the data shifting and pattern generation /detection systems can be synchronised to enable an effective test to be performed at PCB and even system level (see figure 1).

With this basic structure in place software tools can be used to process the JTAG device models (known as BSDL files) plus the netlist(s) of the pcb(s) to generate scan path infrastructure tests, and structural tests for the interconnects between boundary-scan devices. Specific functional logic (so-called 'cluster') tests can be added for testing peripheral non-JTAG elements of a design (memories, communications drivers etc..)

This system has worked well for many designs and continues to be applicable for the majority of mainstream requirements where parallel bus communications is the norm. However new computer architectures utilising busses such as PCI-Express and ATCA for example present new test challenges.

To attain (and often exceed) the speed of parallel busses, these new busses use high-speed serial interfaces and feature differential signal pairs, critical termination components as well as AC-coupling. In all a significant departure from the regular single conductor interconnects of VME or PCI. Attempting to test these circuit connections with the IEEE std. 1149.1 (dot 1) techniques would inevitably lead to disappointing results and most likely false fails. The reason for this being that the standard EXTEST command within dot 1 essentially produces just 'static' or DC patterns at a speed which is highly variable according to the individual design.

Fortunately the demand for testing this type of 'next generation' bus system was anticipated by one of the working parties partaking in IEEE Std 1149 development and as a result the variant IEEE Std 1149.6 (or popularly 'dot 6') was conceived.



IEEE Std.1149.6 (aka ‘Dot 6’) explained.

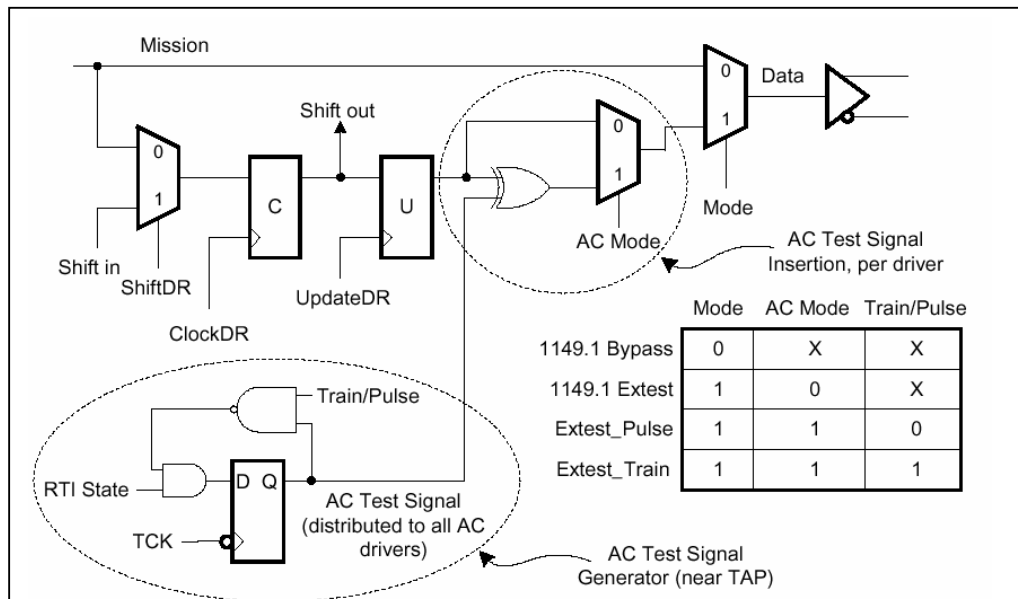
So-called ‘at speed’ testing is very important for fault tolerant technologies such as LVDS – (low voltage differential signalling) which is now used extensively in ‘intra-system communications’ and can be an effective replacement for parallel, back-plane busses.

Faults such as missing terminators and shorts between –ve & +ve signal pairs can often only be detected using so called ‘at-speed’ test techniques. Even a single channel short to VCC or GND may be undetected by a conventional (Dot 1) test due the very high CMRR that these busses afford. Dot 6 allows ICs to have defined both DC ‘testable’ and AC ‘testable’ pins.

The basic concept of Dot 6 is that the ‘transitions’ that form the pulse of the original waveform can always be detected at the receiver, and from this the digital signal the 0 and 1 values can be reconstructed given the appropriate receiver logic. Therefore a time-varying signal must be used that can pass through the AC-coupling when in AC test mode.

The Dot 6 standard defines both the logic to drive a pulse or a pulse train on AC output pins and the logic to detect signal transitions on the AC input pins.

The pulse or pulse train can be selected by two new instructions that are defined in Dot 6 called EXTEST_PULSE and EXTEST_TRAIN respectively. These instructions cause the AC outputs to change state at least 2 times after entry in the Run-Test / Idle (RTI) mode of the TAP controller state machine. The generation of additional transitions on AC driver pins is controlled by entry to and exit from the RTI mode/state. The additional transitions guarantee that the test receiver will have transitions to detect. The transition direction is always relative to the value in the driver boundary-scan register cell, so that the test receiver can recover the test data value (see box-out 1).

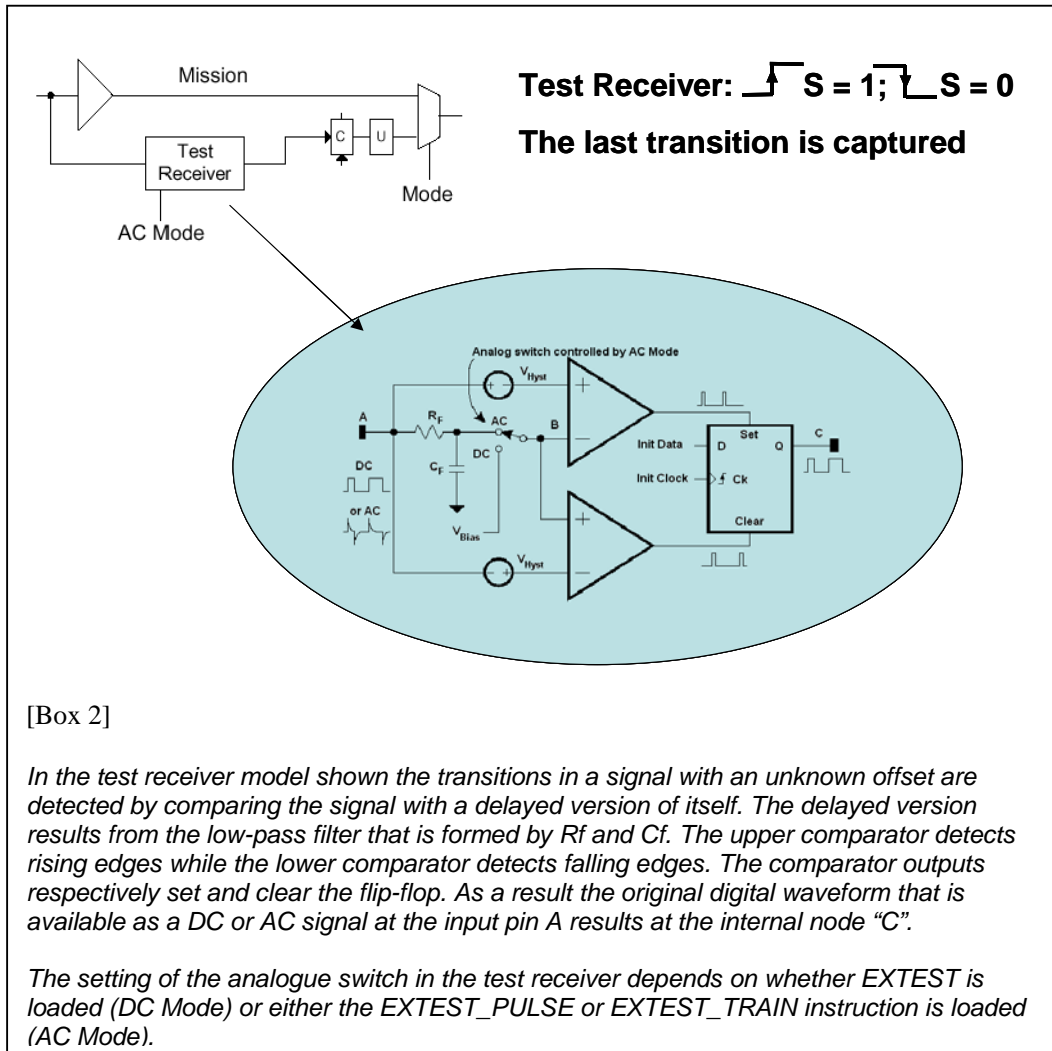


[Box 1]

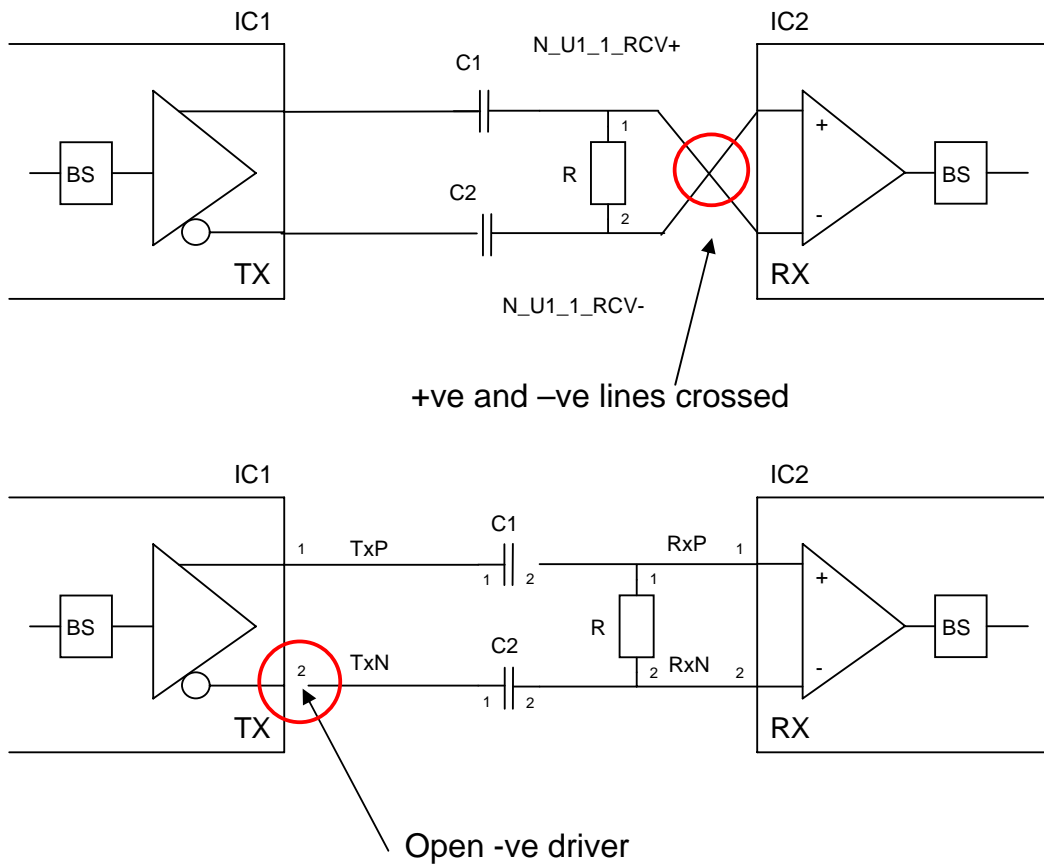
The test logic for an AC pin driver consists of a Dot 1 boundary-register cell (BC_1 in this example) with an extra multiplexer in the test data path. The mode signal selects between the normal ‘mission’ signal or test data. The content of the Update register is transferred to the pin when the EXTEST instruction is loaded (DC Mode). When the EXTEST_PULSE or EXTEST TRAIN instruction is loaded (AC Mode), the pin toggles between the content of the Update register and its inverse value as controlled by the AC Test Signal and the exclusive-OR (i.e the content of the Update register modulated by an exclusive-OR gate with the AC Test Signal is then transferred to the pin).

Only a single AC Test Signal Generator is needed in a chip since the AC Test Signal is distributed to all AC drivers in the chip.

The test logic for an AC pin receiver consists of a Dot 1 boundary-scan register cell with an extra Test Receiver. When EXTEST_PULSE or EXTEST_TRAIN is loaded (AC Mode) the Test Receiver detects transitions of the AC signal seen at the input and determines if this represents a logic “0” or a logic “1”. A signal transition from high to low is stored as a logic “0” ($\searrow S = “0”$); a signal transition from low to high is stored as a logic “1” ($\nearrow S = “1”$). When EXTEST is loaded (DC Mode) the Test Receiver is “transparent” and the input signal level is detected and transferred by the Test Receiver to the boundary-scan register cell (capture flip-flop). See box-out 2



To support the burgeoning market for testing high-speed interconnects JTAG Technologies introduced support for ‘Dot6’ compliant circuits and ICs within a recent release of the acclaimed ProVision application development tool. What’s more the user gets not just a simple GO/NO-GO test result but uniquely precise diagnostics of more than a dozen fault conditions which could occur on a regular differential signal network. The diagrams below indicate just 2 common fault types that without ‘Dot6’ testing would prove difficult. These faults were implemented on a National Semiconductor ‘Dot6’ evaluation design featuring their SCAN90CP02 LVDS cross-point switch.



1149.6 – Example Possible Defects

Conclusion – low-cost and effective

In conclusion it can be seen that a combined effort from one of the electronics industries' professional bodies, silicon vendors some of the more prevalent test equipment suppliers has introduced a timely solution to the vexing issue of testing high-speed interconnects. By using a method based firmly on the tried and tested technique of IEEE Std 1149.1 boundary-scan, structural board and system testing including precise fault diagnostics can be applied to today's high-speed serial bus structures, painlessly and via the embedded test logic within the system devices themselves.

The result is a low cost method relying more on software tools than sophisticated tester hardware which can be applied to any compliant design with a minimum of design effort.