DFT Checklist

ITEM	ADDRESSED? (Yes/No, description)
General Information:	
Block Name	
Est. gate count (gates/flops):	
Clock domains/frequencies	
Clock Inputs (name/off-state/external source):	
Reset Inputs (name/off-state):	
Registers at boundaries:	
Safe digital scan-mode values driven at digital → analog boundary?	
Reviewed with analog team?	
Document scan-conditioned signals	
Immediately registered Incoming signals at analog → digital boundary	
Uncovered combinational logic	
Testmode input muxing	
PLL bypass	
functional injection points	
Any others (list)	
Scan mode used to gate clock/resets	
Observation testpoints	
Analog testpoints	
Clock output muxes	
Block Bypasses	
Analog block bypasses (for calibration):	
Initialization	
Sequential logic resetable	
Sequential flush method (specify):	
Design Practice Avoidance	
Asynchronous logic	
Logic redundancy	
Delay dependent Logic	
Asynchronous self-resetting logic	
Data mixed with clock	
Tri-state buses	
Scan Design	
Full scan? (list un-scanned logic)	
Block-level test coverage	
At-speed scan supported?	
Transition delay test coverage	
Test Compression supported?	
Block-level chain length	
Number of scan chains	
Sense of 1st and last clocks	
Pin constraints	

- False/multicycle paths?
  - SDC file transferred to DFT
- Synthesis
  - Standard scripts used
  - DFT DRCs (list deviations)
  - Document scan-conditioned signals

Scan practices

- Clocks
  - Controlled from primary input
  - Gated in scan mode
  - Negative edge flops
  - Clock relationships
  - FIFOs?
- Resets
  - Controlled from primary input
- Memory (in scan mode)
  - Shadow logic covered
  - Control signals handled in scan mode

Embedded Memory (testing of)

- Memory instances
- BISTed memories
- Self-repairable memories
- Non-BISTed memories
- Custom memory test? (list)

Embedded IP

- Examined against all DFT reqs
- Scan models available
- Memory Scan/BIST models available
- Simulation models available